Institute of Modern Physics
Chinese Academy of Sciences

High Intensity Heavy-ion Accelerator Facility

FPGA-based digital IQ demodulator used in the beam position monitors for HIAF-BRing

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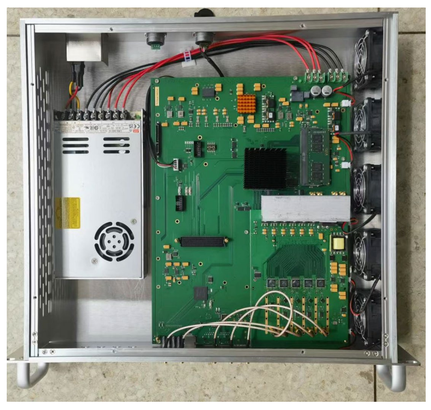
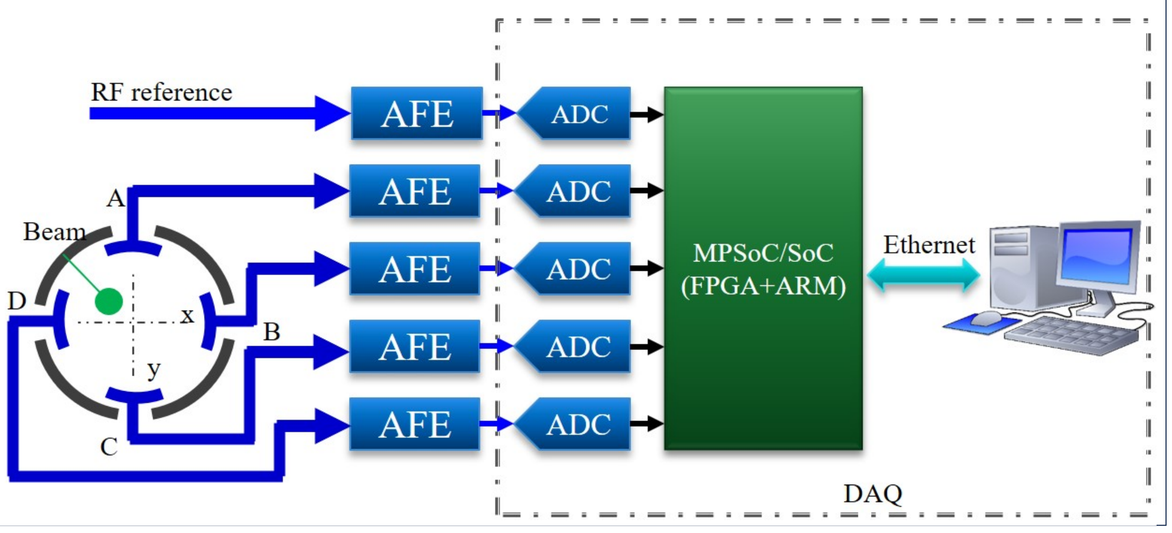
Introduction

Beam Position Monitor (BPM) is a common non-intercepted beam measurement device used to measure the lateral position of beams in vacuum tubes and is widely used in cyclotrons, linear accelerators, and synchrotron. In HIAF, 40 BPM will be allocated around the BRing and the resolution of the BPM should be better than 0.1 mm. A fully digital developed prototype is designed for the beam position measurement system. The prototype of the BPM algorithm was tested and evaluated on HIRFL-CSRm which has a close revolution frequency range.



System Architecture

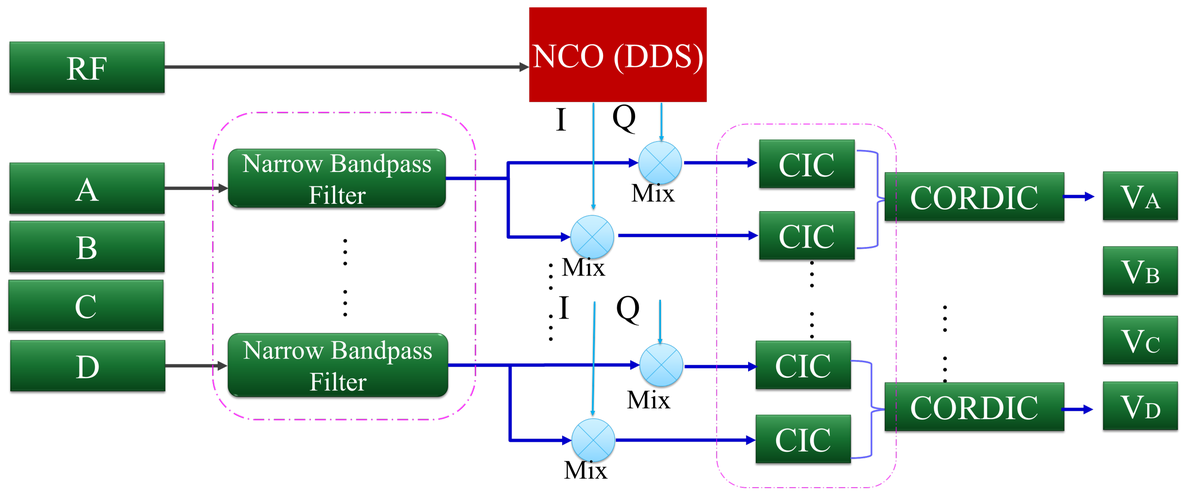
The signal on the pick-up first passes through the front-end amplifier with a gain of about 40 dBm and then travels over a long coaxial cable to the BPM data processing electronics and data acquisition system. In the BPM electronics, high-speed ADCs (analog to digital converter) are employed, and the sample rate is 250 Msps. The main digital signal processor is implemented by a System-on-Chip (SoC) device ZYNQ UltraScale+(ZU15) series. By using the SoC, the data from FPGA to ARM could be easily acquired. FPGA is mainly used to implement the beam position calculation process, and ARM is responsible for converting the data from FPGA, running the embedded the Linux systems and the EPICS PVs over the network.



Digital Signal Processing

The sampling frequency of 250 MHz is the main clock frequency in the FPGA. After the ADC sampling the amplified signal from pick-ups, the acquired signal is first passed through a narrow band-pass filter that cuts off high- and low-frequency components to ensure that the position calculation process is as unaffected as possible. Since the charged particles in the synchrotron pass through the Radio Frequency (RF) cavity to obtain energy and are accelerated, the RF signal is synchronized with the charged particles. The RF signal is also been acquired. In this design, the RF signal is used to obtain the revolution frequency in real time to generate the orthogonal components of the digital demodulator.

- Narrow bandpass filter 0.2 MHz ~ 2 MHz (IIR + FIR)
- NCO (Numerical controlled oscillator) realized by DDS (Direct Digital Synthesizer), generates In-phase and Quadrature components
- CIC filter to decrease the data rates and get the DC component mixed signal
- CORDIC algorithm calculate the channel amplitude
- Different over sum



$$x = x_{offset} + kx_1 \frac{VA - VC}{VA + VC} + kx_2 \left(\frac{VA - VC}{VA + VC}\right)^2$$

$$y = y_{offset} + ky_1 \frac{VB - VD}{VB + VD} + ky_2 \left(\frac{VB - VD}{VB + VD}\right)^2$$

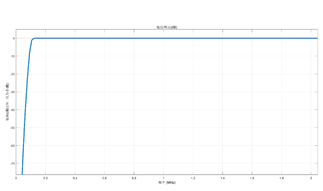
Test Results

Laboratory Test Result

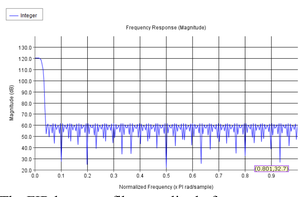
Ultra-Narrow Band Filter Design

$$H(z) = \frac{\sum_{r=0}^{M} b_r z^{-r}}{1 - \sum_{k=0}^{N} a_k z^{-k}} \pi r^2$$

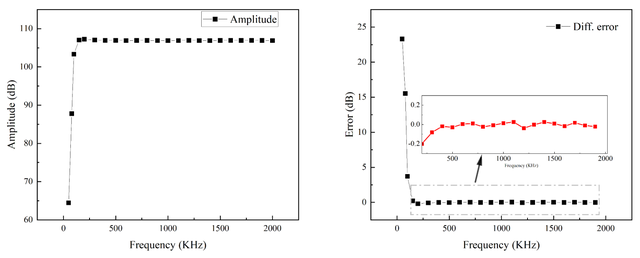
The sampling rate is 250 Msps in this design. The revolution frequency of HIAF-BRing is from 0.2 to 1.78 MHz. An ultra-narrow band-pass filter with a frequency in the range of 0.17 ~ 2.5 MHz is necessary. Compared to the ADC sample frequency, the revolution frequency of the synchrotron is located in the low-frequency sideband. In this design, a band-pass filter is designed by combining an FIR low-pass filter and an IIR high-pass filter.



Matlab IIR filter amplitude-frequency response

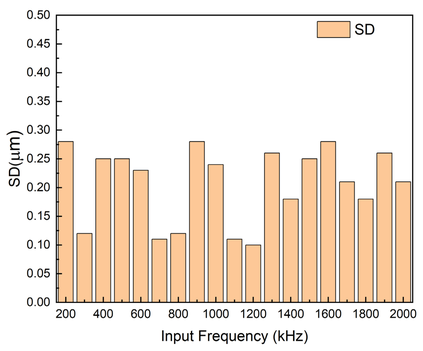


The FIR low-pass filter amplitude-frequency response

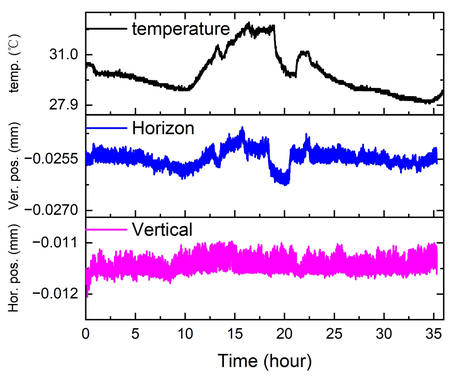


IIR filter amplitude-frequency response in FPGA

The standard deviation tested under different input frequency

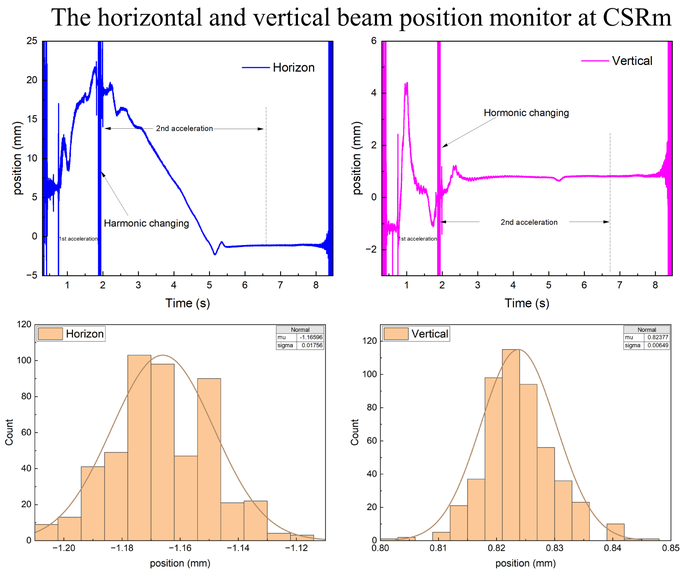


Long term stability in laboratory

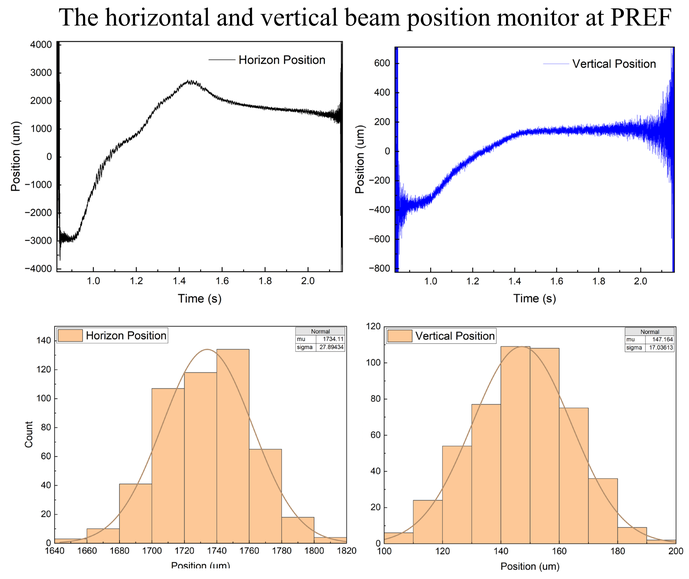


HIRFL CSRm && PREF Test Results

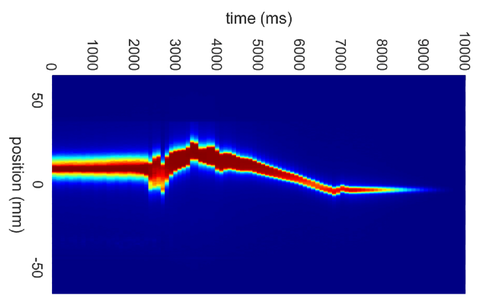
The horizontal and vertical beam position monitor at CSRm

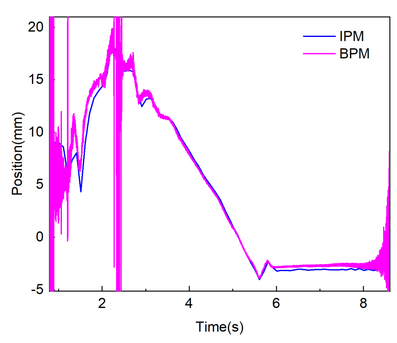


The horizontal and vertical beam position monitor at PREF



Compare with the noninvasive Ionization Profile Monitor (IPM)





The newly developed BPM prototype has been tested in the laboratory and with the beam as well. By employing the digital IQ demodulator, the amplitude of each pick-up relative amplitude is retrieved. The RF signal is essential for the NCO to generate the I and Q components in digital real-time. An ultra-narrow bandpass filter which combines an IIR high pass filter and an FIR low pass filter is designed. The laboratory test results show that the resolution of 0.3 μm when the input signal power is -25 dBm and the long-term stability is below 5 μm when the temperature changes. The online beam test comparison shows that the BPM-calculated beam position could match the IPM-detected beam profile results. The resolution of the tested BPM at field is better than 30 μm which meets the requirements.

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FUTURE WORK

- Code optimization for SoC platform about algorithm in the FPGA
- Embedded EPICS systems and application software
- Long-term test the behavior of this prototype in HIRFL-CSRm